

REMARKS

Amendment made to claim 1

Claim 1 has been amended to correct a typographical error in the claim as originally presented. In particular, the term “threshold” within the phrase “to execute the threshold” is correctly the term “code section.” Applicant regrets and apologizes for this error.

Claim rejections under 35 USC 101

Claim 20 has been rejected under 35 USC 101 as being directed to non-statutory subject matter. In particular, the Examiner has submitted that because claim 20 delineates that the computer-readable medium can be “a modulated carrier signal,” the claim can be directed to an intangible computer-readable medium. Applicant does not necessarily agree, but in good faith to advance the present patent application to allowance, Applicant has amended claim 20 so that it cannot be directed to a computer-readable medium that is a modulated carrier signal. As such, Applicant requests the withdrawal of this rejection.

Claim rejections under 35 USC 112

Claims 1-10 have been rejected under 35 USC 112, second paragraph, as being indefinite. In particular, the Examiner states that the term “approach” in these claims is “a relative term which renders the claim indefinite.” (Office action, p. 3) Furthermore, the Examiner has stated that the “term ‘approach’ is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.” (Id.) Applicant respectfully but firm disagrees with the Examiner.

First, the term “approach” is not a “relative” term. It is being used as a noun (i.e., not as a verb) in claims 1-10; Applicant surmises that this may be the basis of the Examiner’s potential confusion as to how this term is being used in the claims. There are two different approaches

delineated in claims 1-10: a “software approach to locking memory” and a “hardware approach to transactional memory.” The former is an approach to locking memory that is software in nature, due to the adjective “software.” The latter is an approach to transactional memory that is hardware in nature, due to the adjective “hardware.”

Furthermore, the online dictionary www.dictionary.com defines the noun “approach” as follows: “the method used or steps taken in setting about a task, problem, etc.: His approach to any problem was to prepare an outline.” The online thesaurus www.thesaurus.com relevantly provides the following synonyms to the noun “approach”: manner, method, procedure, and technique. Applicant notes that one of ordinary skill within the art uses the ordinary meaning of terms in the claims unless the specification provides a contrary definition. *Toro Co. v. White Consol. Indus., Inc.*, 199 F.3d 1295, 1299, 53 USPQ2d 1065, 1067 (Fed. Cir. 1999) (“[W]ords in patent claims are given their ordinary meaning in the usage of the field of the invention, unless the text of the patent makes clear that a word was used with a special meaning.”).

Applicant is using the noun “approach” within claims 1-10 consistent with its ordinary meaning as provided by the online dictionary www.dictionary.com and the online thesaurus www.thesaurus.com. The term “approach” is used to mean “the method used to set about a task,” and as such is a “manner, method, procedure, [or] technique” that is used to set about a task. The task in question as to the software approach is the task of locking memory. The task in question as to the hardware approach is the task of implementing or effecting transactional memory.

The Examiner has stated that the specification does not provide “a standard for ascertaining the requisite degree” of the term “approach.” However, there is no “degree” as to the noun “approach.” Applicant surmises that the confusion may lie in the Examiner’s interpretation of the term “approach” as a verb, such as “Bob approaches Bill,” where the degree in this example would be “how closely does Bob advance towards Bill.” In the usage of the

present claims, however, the term “approach” is not a relative term, and as such does not have any “requisite degree” that needs to be ascertained.

Furthermore, Applicant notes that the specification utilizes the terminology “approach” consistent with its ordinary meaning as a noun as the method used in setting about a task, a procedure, a manner, or a technique. Paragraph 9 of the patent application as filed, for instance, states that “[o]ne approach to ensuring that a number of transactions are not attempting to process the same memory at the same time is to use a software locking approach,” where the rest of paragraph 9 describes what such a software locking approach entails. Likewise, paragraph 10 of the patent application as filed states that “[a]nother approach to ensuring that a number of transactions are not attempting to process the same memory at the same time is to use a hardware transactional memory approach,” where the rest of paragraph 10 describes what such a hardware transactional memory approach entails. Therefore, the Examiner is incorrect in stating that “one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.”

Applicant notes that “a claim term that is not used or defined in the specification is not indefinite if the meaning of the claim term is discernible.” (MPEP sec. 2173.02, citing *Bancorp Services, LLC v. Hartford Life Ins. Co.*, 359 F.3d 1367, 1372, 69 USPQ2d 1996, 1999-2000 (Fed. Cir. 2004)) Here, the meaning of the claim term “approach” is indeed discernible. The term is being used in relation to its ordinary meaning as a noun, as has been discussed above. Therefore, this term is definite under 35 USC 112, second paragraph.

The Examiner has suggested that Applicant replace the terminology “software approach” in the claims with “method using software” and the terminology “hardware approach” with “method using hardware”. However, this suggestion makes the claim language unclear. For example, the claim would read “a method using software to locking memory” and “a method using hardware to transactional memory,” both of which are incongruous. Applicant further notes that “if the language used by applicant satisfies the statutory requirements of 35 USC 112, second paragraph, but the examiner merely wants the applicant to improve the clarity or precision of the

language used, the claim must not be rejected under 35 USC 112, second paragraph, rather, the examiner should suggest improved language to the applicant.” (MPEP sec. 2173.02) In the present patent application, therefore, the rejection under 35 USC 112, second paragraph is improper, since the claim language already satisfies the statutory requirements of definiteness. Moreover, the Examiner’s suggested language renders the claim language unclear – for instance, the phrase “a method using hardware to transactional memory” does not make sense.

For all of these reasons, Applicant traverses the rejection under 35 USC 112, second paragraph. The Examiner is respectfully encouraged to contact Applicant’s representative, Mike Dryja, at the phone number listed below, if further explanation is needed as to the terminology “approach” as used in claims 1-10.

Claim rejections under 35 USC 102

Claims 1-20 have been rejected under 35 USC 102(b) as being disclosed by Paya (6,993,663). Applicant respectfully but very firmly traverses this rejection for the following independent and separate reasons, each of which are introduced under a separate heading in *italics*.

Prima facie anticipation has not been shown

The sum total of the explanation of the rejection of all the claims 1-19 over Paya in the Office Action is as follows. For each claim, the Examiner recites the claim language in question, and then simply inserts “(col. lines 11-57)” – apparently referencing column 4, lines 11-57 in particular¹ – at the end of the claim language as the entire “explanation” as to how Paya discloses this claim language. Such a rejection very much fails the responsibility of the Examiner to furnish a *prima facie* case of anticipation. The Examiner is aware that “[i]t is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office.” In re Skinner, 2 USPQ2d 1788 (BPAI 1986). Under 35 USC 102, every limitation of a claim must identically appear in a single prior art reference for it to anticipate the claim. In re Bond, 15 USPQ2d 1566 (Fed. Cir. 1990). Most significantly, the Federal Circuit expects the Patent and Trademark Office’s “anticipation analysis [to] be conducted on a limitation by limitation basis, with specific fact findings for each contested limitation and *satisfactory explanations* for such findings.” *Gechter v. Davidson*, 43 USPQ2d 1030 (Fed. Cir. 1997) (Emphasis added). “Claim construction must also be explicit . . .” *Id.*

Applicant respectfully but strongly asserts that the Examiner has failed to provide a *prima facie* case of anticipation to which Applicant can properly respond.. The Examiner in the Office Action has simply delineated the limitations of claims 1-19 and then summarily without any analysis or explanation concludes that Paya anticipates these limitations in “col. 4 lines 11-57,” without providing any explanation as to which elements in Paya correspond to which elements or limitations of the invention. Paya is a complex reference, and Applicant can only guess which elements the Examiner intends to correspond with which limitations of the claims.

¹ In the text of the office action, no column number is listed. However, the Examiner has indicated to Applicant’s representative, Mike Dryja, that the column number intended was column 4. Therefore, in the remainder of the office action response, Applicant presumes that the Examiner intended column 4, lines 11-57 when referencing “col. lines 11-57” of Paya.

However, determining which elements of Paya correspond to which limitations of the claims is not Applicant's obligation – it is the Examiner's obligation to provide an anticipation analysis on a limitation by limitation basis, as indicated in the *Gechter* decision, to warrant a *prima facie* case of anticipation. Indeed, 37 CFR 1.106(b) notes that “[w]hen a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated *as nearly as practicable*.” (Emphasis added) However, the Examiner has not designated which parts of Paya correspond to the various limitations and elements of the claims. The Examiner has just stated that “col. 4 lines 11-57” of Paya disclose every limitation of each of claims 1-19. The Examiner has made no attempt at claim construction either.

Therefore, Applicant strongly submits that the Examiner has failed to provide a *prima facie* case of anticipation of the claims in questions as to Paya. The completely conclusory nature of the Examiner's rejection contains no analysis, and no indication where in Paya the Examiner finds the limitations and elements of the claimed invention. The Examiner should surely recognize that this rejection would easily not be upheld on appeal.

Independent claim 1 is not anticipated by Paya

Applicant next asserts that independent claim 1 in particular is not anticipated by Paya. Claim 1 is limited to “a software approach to locking memory” in order to execute a code section, and that employs “a pseudo-transaction” to determine whether “a hardware approach to transactional memory” in order to execute the code section would have been successful. Where this “hardware approach to transactional memory” to execute the code section satisfies “a threshold based on success of at least the pseudo-transaction,” the hardware approach is subsequently utilized to execute the code section.

Applicant has reviewed Paya in detail, including lines 11-57 of column 4 of Paya, and as it is understood by the Applicant, Applicant cannot find any reference in Paya to any type of software approach to locking memory, any type of pseudo-transaction, or to any type of hardware

approach to transactional memory. The terms “lock” or “locking,” “transaction” or “transactional,” and “pseudo” appear nowhere in Paya, such that it is difficult to even imagine how Paya can anticipate a claim that is specifically limited to a software approach to “locking memory,” a hardware approach to “transactional memory,” and such a software approach that employs a “pseudo-transaction.” A prior art reference must disclose each element of the claimed invention “arranged as in the claim.” (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)) Here, Paya does not disclose any approach to locking memory or transactional memory, let alone a software approach to locking memory that employs a pseudo-transaction to determine whether a hardware approach to transactional memory would be successful in executing a code section, as in the claimed invention. Indeed, Paya is directed completely to “preventing input data buffer overrun” (see Title and Abstract, for instance). Such buffer overrun prevention as described in Paya does not have anything to do with utilizing a software approach to locking memory that employs a pseudo-transaction to determine whether a hardware approach to transactional memory would successfully execute a code section.

Applicant therefore requests that the Examiner specifically discuss what elements of Paya correspond to the “software approach to locking memory,” the “pseudo-transaction” used by this software approach, “the hardware approach to transactional memory,” and the “threshold based on success of at least the pseudo-transaction” against which the hardware approach is tested. Indeed, as has been discussed above, it is the Examiner’s obligation in presenting a *prima facie* case of anticipation to provide this explanation of Paya vis-à-vis the claimed invention. That is, the Federal Circuit expects the Patent and Trademark Office’s “anticipation analysis [to] be conducted on a limitation by limitation basis, with specific fact findings for each contested limitation and *satisfactory explanations* for such findings.” *Gechter v. Davidson*, 43 USPQ2d 1030 (Fed. Cir. 1997) Here, the Examiner has simply said that lines 11-57 of column 4 of Paya disclose all the elements of claim 1 (as well as every other claim), without providing any

explanation as to how the elements of Paya “line up with” (i.e., disclose) the limitations of the claimed invention.

Independent claim 11

Applicant also asserts that independent claim 11 in particular is not anticipated by Paya. Claim 11 is limited to a “processor having transactional memory capability, including a pseudo-transactional memory capability that determines whether the transactional memory capability would have been successful.” Claim 11 is further limited to a “memory storing a spin lock function to execute a code section by utilizing the transactional memory capability upon the transactional memory capability having satisfied a threshold based upon success of at least the pseudo-transactional memory capability.”

Applicant has reviewed Paya in detail, including lines 11-57 of column 4 of Paya, and cannot find any reference to Paya to a processor having transactional memory capability, including a pseudo-transactional memory capability, nor to a spin lock function to execute a code section by utilizing the transactional memory capability upon this capability having satisfied a threshold based upon success of at least the pseudo-transactional memory capability. None of the terms “lock,” “locking,” “spin lock,” “transaction,” “transactional,” and “pseudo” appear anywhere in Paya, such that it is difficult to image here, too, how Paya can anticipate a claim that is specifically limited to a spin lock function to execute a code section by utilizing the transactional memory capability upon this capability having satisfied a threshold based upon success of at least the pseudo-transactional memory capability. A prior art reference must disclose each element of the claimed invention arranged as in the claim. Here, Paya does not disclose in any way whatsoever a spin lock function executing a code section by utilizing the transactional memory capability upon this capability having satisfied a threshold based upon success of at least the pseudo-transactional memory capability. As has been noted in relation to claim 1 above, Paya is directed completely to preventing input data buffer overrun, which as described in Paya does not have anything to do

with a spin lock function executing a code section by utilizing the transactional memory capability upon this capability having satisfied a threshold based upon success of at least the pseudo-transactional memory capability.

Applicant therefore requests that the Examiner specifically discuss what elements of Paya correspond to the “transactional memory capability” of the processor, the “pseudo-transactional memory capability that determines whether the transactional memory capability would have been successful,” and the “spin lock function to execute a code section by utilizing the transaction memory capability upon the transactional memory capability having satisfied a threshold based upon success of at least the pseudo-transactional memory capability.” It is the Examiner’s obligation in presenting a *prima facie* case of anticipation to provide this explanation of Paya vis-à-vis the claimed invention. Anticipation analysis is to be conducted in a limitation-by-limitation basis, with specific fact findings for each limitation and *satisfactory* explanations for such findings. Here, the Examiner has simply stated that lines 11-57 of column 4 of Paya disclose all the elements of claim 11 (as well as every other claim), without providing any *explanation* as to how the elements of Paya disclose the limitations of the claimed invention, as arranged in claim 11.

Independent claim 17

Applicant finally asserts that independent claim 17 in particular is also not anticipated by Paya. Claim 17 is limited to “utilizing a hardware approach to transactional memory to execute a code section.” This utilization is performed “after having utilized a software approach to locking memory to execute the code section and the hardware approach to transaction memory having satisfied a threshold based at least upon a pseudo-transaction to determine whether the hardware approach would have succeeded in executing the code section.”

Applicant has reviewed Paya in detail, including lines 11-57 of column 4 of Paya, and cannot find any reference to Paya to any type of locking memory, any type of pseudo-transaction, or to any type of hardware approach to transactional memory. The terms “lock” or “locking,”

“transaction” or “transactional,” and “pseudo” appear nowhere in Paya, such that it is difficult to image here, too, how Paya can anticipate a claim that is specifically limited to a software approach to “locking memory,” a hardware approach to “transactional memory,” and an approach that employs a “pseudo-transaction.” A prior art reference must disclose each element of the claimed invention arranged as in the claim. Here, Paya does not disclose any approach to locking memory or transactional memory, let alone employment of a pseudo-transaction to determine whether a hardware approach to transactional memory would be successful in executing a code section, as in the claimed invention. As has been noted in relation to claim 1 above, Paya is directed completely to preventing input data buffer overrun, which as described in Paya does not have anything to do with utilizing a software approach to locking memory, and employing a pseudo-transaction to determine whether a hardware approach to transactional memory would successfully execute a code section.

Applicant therefore requests that the Examiner specifically discuss what elements of Paya correspond to the “software approach to locking memory,” “the hardware approach to transactional memory,” and the “threshold based at least upon a pseudo-transaction” to determine whether the hardware approach would have succeeded in executing a code section. It is the Examiner’s obligation in presenting a *prima facie* case of anticipation to provide this explanation of Paya vis-à-vis the claimed invention. Anticipation analysis is to be conducted in a limitation-by-limitation basis, with specific fact findings for each limitation and *satisfactory* explanations for such findings. Here, the Examiner has simply stated that lines 11-57 of column 4 of Paya disclose all the elements of claim 17 (as well as every other claim), without providing any *explanation* as to how the elements of Paya disclose the limitations of the claimed invention, as arranged in claim 17.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mike Dryja, Applicants' Attorney, at 425-427-5094, so that such issues may be resolved as expeditiously as possible. For these reasons, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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